UNITED STATES PATENT AND TRADEMARK OFFICE

A/D

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/689,442	10/12/2000	Loren T. Lancaster	NVX-0015C1	7388

7590 08/14/2002

Bradley T. Sako
3954 Loch Lomand Way
Livermore, CA 94550

EXAMINER
PIERRE, KENELT

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/689,442	LANCASTER, LOREN T.	
	Examiner	Art Unit	
	KEN PIERRE	2822	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 to 69* is/are pending in the application.

4a) Of the above claim(s) *1 to 48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *49 to 68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This is in response to the applicant's amendments and arguments received on July 19, 2002. After a complete review of the response and claims, Applicant's arguments have been fully considered and have not found persuasive.

Applicant argues that: "Chang does not show a gate of a first conductivity type and source and drain regions of a second conductivity type." "The charge storing structure is not made of (silicon oxide, or a combination of silicon oxide and nitride)." Chang uses a polysilicon floating gate 30 is provided on the tunneling oxide 28, and an inter-gate dielectric 32 separates floating gate 30 from control gate 34 (Col. 1; line 55 to 60). A p-type substrate 40 and n+ type source/drain regions 42, 44 (Col. 1; line 59 to 68). If a polysilicon gate is used instead of a metal gate, the polysilicon must be doped with a different conductivity type than the source/drain, that inversion and accumulation occur at different voltage. The inter-gate dielectric 116 (usually silicon oxide, or a combination of silicon oxide and nitride) and control gate 118, is formed on dielectric layer 110. This inter gate dielectric, which separates the floating gate from the control gate holds the bulk of the charge that is injected into the floating gate. The floating gate 114 is sufficiently conductive so that injected electrons can redistribute themselves (Col. 6, line 60 to 67).

Regarding 57 to 59, Vinal clearly teaches how to avoid introducing contact potential as part of the threshold voltage. A semiconductor device with N channel FETs requires P-polysilicon gate, and P channel FETs require N-polysilicon gate. N channel

means P well, P tub or P substrate. P channel means N well, N tub or N substrate. A significant contact potential exists between metal gate and P++ semiconductor material, and it is necessary to avoid introducing this contact potential as part of the threshold voltage. Therefore, poly gates with unmatched doping with the source and drain are used (Col. 7; line 16 to 25).

Regarding 60 to 69, when a bias is applied to the gate of a device depending on the polarity of the signal it either produces in accumulation of charges at the silicon/oxide

interface or a depletion of charge at the silicon/oxide interface. For a memory device, which is based on the same principles of MOS capacitor accumulation usually means "write". When a write bias is applied for predetermined period of time, it increases the accumulation of charge (Col.5; line 46 to 49).

Therefore, the rejection mailed on April 24, 2002 remains.

Election/Restrictions

2. Claims 1 to 48 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a non-elected group, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 2. Claims 1 to 48 are cancelled as requested by applicant. Claims 49 to 69 are pending.

Claim Objections

3. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 65-68 have been renumbered 65-69, due to two claims 65.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 49 to 56 and 59 are rejected under 35 U.S.C. 102(b) as being anticipated by Chang (4,958,321)

Regarding claim 49, Chang discloses a device (Col. 1; line 25 to 30) with a Double-Polysilicon Technology. (Col. 1; line 59 to 68) (FIG.1) (FIG.2) It includes a p-type substrate 40 and n+ type source and drain regions 42, 44. A tunnel oxide layer 46, having a thickness of approximately 200 Angstroms, is provided on the surface of the substrate 40 under a floating gate 48.This transistor is controlled by control gate.

Regarding claims 51, 52, 54 to 56 (Col. 4; line 55 to 60) a floating gate is provided on the dielectric layer, an inter-gate dielectric provided on the floating gate, and a control gate provided on the inter-gate dielectric. (Col. 8; line 61 to 63) (FIG.4) An oxide is grown thermally on the surface of substrate 100. (Col. 6; line 58 to 67) The floating gate 114 is formed of a semiconductor material, for example, lightly doped polysilicon. (Col. 7; line 16 to 25) The actual doping level of polysilicon film is related to the stated fabrication techniques and equivalents thereof because the polysilicon film resistivity is determined by the number of built-in electrons and their mobilities. The doping level of polysilicon film depends on how less resistive the polysilicon film is to be for its use in a device.

Regarding claim 53, (Col. 7; line 65 to 68) The gate structure 119, including floating gate 114, inter-gate dielectric 116 (usually silicon oxide, or a combination of silicon oxide and nitride) and control gate 118, is formed on dielectric layer 110.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 57 to 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (4,958,321) in view of Vinal (4,990,974)

Regarding claims 57 to 59, Chang discloses a device (Col. 1; line 25 to 30) with a Double-Polysilicon Technology. (Col. 1; line 59 to 68) (FIG.1) (FIG.2) It includes a p-type substrate 40 and n+ type source and drain regions 42, 44, with floating and control gates.

However, Chang do not disclose that the control poly gate is of opposite conductivity doping type to the source and drain doping.

Vinal discloses (Col. 7; line 16 to 25) (FIG. 10B; 10D) a semiconductor device where N channel FETs require P-polysilicon gate, and P channel FETs require N-polysilicon gate. A significant contact potential exists between metal gate and P++ semiconductor material, and it is necessary to avoid introducing this contact potential as part of the threshold voltage. Therefore, poly gates with unmatched doping with the source and drain are used.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a control gate poly with opposite conductivity type to the source and drain conductivity type because a significant contact potential exists between metal gate and P++ semiconductor material, and it is necessary to avoid introducing this contact potential as part of the threshold voltage, as taught per Vinal reference.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 60 to 63 are rejected under 35 U.S.C. 102(b) as being anticipated by Lancaster et al (5,774,400)

Regarding claims 60 to 63, Lancaster et al disclose (ABSTRACT) a method and structure for preventing erasure in a non-volatile memory device. (Col. 7; line 9 to 13) An external power source 120 supplies voltage Vpp between the gate 44 at contact 110 and to the substrate 40 at least at point 130 to create internal electric fields. (Col.5; line 34 to 40) The transistor is placed on silicon substrate of a first conductivity type, and includes source and drain junctions of a second conductivity type, a conductive control gate, and a charge accumulation layer residing at least between portions of the control gate and the substrate. (Col. 10; line 10 to 13) Gate or charge depletion layers are also present the device operation. (Col.11; line 4 to 8) The device first node or first layer comprises a memory transistor channel. The second node or second layer comprises said memory transistor gate.

Regarding claims 64, 65, 67 and 68, (Col.5; line 46 to 49) when a write bias is

applied for predetermined period of time, it increases the accumulation of charge. (Col.5; line 45 to 46) The tunneling current from both sources are designed to be a function of the accumulated charge, each affected in an opposite way to the other. (Col.2; line 65 to 67) (FIG. 2 diagram labeled "Direct Tunneling") Current 201 tunnels from the channel region 30 tunnel completely through silicon dioxide layer 41 directly into the silicon nitride 42. (Col. 7; line 2 to 5) (FIG. 1) The transistor structure 10 comprising a silicon substrate 40 which includes source 45 and drain 46 junctions bordering a transistor channel 30 that resides substantially at the substrate surface. (Col. 7; line 6 to 13) Above the substrate 40 resides a composite structure of a bottom tunnel oxide 41, a charge storage layer 42, a top blocking dielectric 43 and a conductive gate 44. (Col.11; line 29 to 33) The device substrate has a first conductivity type, and source and drain regions have a second conductivity type.

Regarding claims 66 and 69, (Col.11; line 4 to 10) The device charge storage layer comprises silicon nitride, silicon oxynitride a layer of silicon dioxide.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this non-final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed

within TWO MONTHS of the mailing date of this non-final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this non-final action.

8. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Ken Pierre whose telephone number is (703) 305-4002. The examiner can normally be reach on Monday-Friday from 8:30AM to 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Carl Whitehead, Jr. can be reach at (703) 308-4940. The fax telephone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

KP

July 31, 2002

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800